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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PHAN, RAYMOND NGAN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 10/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,805	OSHINS, JACOB	
	Examiner	Art Unit	
	Raymond Phan	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2006*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28-32* is/are allowed.

6)☒ Claim(s) *1-27, 33-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: amendment filed on May 25, 2006.

2. This application has been examined. Claims 1-34 are pending.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-11, 17-18, 21-23, 27 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Laurenti (US No. 6,502,152) in view of Short et al. (US NO. 5,708,814).

In regard to claims 1, 27, Laurenti discloses an interrupt arbitration system, comprising: at least one request associated with an interrupt resource, the request including at least two dimensions related to an interrupt and an interrupt service component (see col. 11, lines 5-11); and at least one arbiter to process the request and return a subset of interrupt resource ranges in view of available system resources (see col. 13, line 57 through col. 14, line 11). But Laurenti does not disclose the request associated with the time component. However Short et al. disclose the delay time value associated with the interrupt request that interrupt controller will delay from the earliest pending interrupt event of the controlled peripheral device before asserting an IRQ to the CPU (see col. 3, lines 50-67) that would reduce the interrupt processing overhead of the CPU. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the

invention was made to have combined the teachings of Short et al. within the system of Laurenti because it would dramatically reduce the interrupt processing overhead of the CPU.

In regard to claim 2, Laurenti discloses further comprising a requesting component that communicates to the arbiter in order to determine available system resources that may be utilized by the requesting component to perform one or more tasks (see col. 13, line 57 through col. 14, lines 11).

In regard to claim 3, Laurenti discloses the system resources are related to at least one of I/O ports, memory locations, DMA channels (Direct Memory Access), bus numbers, and interrupt requests (IRQs) (see table 8).

In regard to claim 4, Laurenti discloses further comprising at least one arbiter for a respective system resource (see col. 18, line 65 through col. 19, line 32).

In regard to claim 5, Laurenti discloses the system resources are associated with one or more system devices, buses, or other components which are negotiated for via the at least one arbiter (see col. 12, lines 28-58).

In regard to claim 6, Laurenti discloses the requesting component issues a multidimensional interrupt request (IRQ) associated with one or more interrupt inputs, signals, or assignments, the IRQ is employed to interrupt at least one processing component (see col. 11, lines 5-11).

In regard to claim 7, Laurenti discloses the interrupt service component is associated with an Interrupt Descriptor Table (IDT) entry that is concurrently mapped with an IRQ (see col. 11, lines 5-19).

In regard to claim 8, Laurenti discloses the IRQ is mapped in accordance with a first request and the IDT entry is mapped in accordance with a separate request (see col. 11, lines 5-19).

In regard to claim 9, Laurenti discloses the arbiter performs an analysis of system resources, and if requested interrupt resources are found to be available, the arbiter returns a resource subset or data packet indicating the interrupt resources that can be utilized by a requesting component (see col. 13, line 56 through col. 14, line 4).

In regard to claim 10, Laurenti disclose if the interrupt resources are not deemed available by the arbiter, a code or flag is returned to the requesting component indicating that requested interrupt resources cannot be satisfied (see col. 19, lines 4-32).

In regard to claim 11, Laurenti discloses the request further comprising at least one other dimension including a time component (i.e. priority) (see col. 17, line 56 through col. 18, line 65).

In regard to claim 17, Laurenti discloses further comprising a control component to tune performance of a machine by influencing interrupt assignment policy (see col. 19, lines 4-53).

In regard to claim 18, Laurenti discloses further comprising a monitor component to provide feedback to the control component regarding system performance (see col. 19, lines 4-53).

In regard to claim 21, Laurenti discloses the interrupt is associated with at least one of a local bus, a system bus, a PCI bus, and an ISA bus (se col. (see col. 4, lines 9-51).

In regard to claim 22, Laurenti discloses the interrupt is at least one of derived from at least two components and coupled to one or more devices that are associated with one or more buses (see col. 12, lines 1-18).

In regard to claim 23, Laurenti discloses further comprising at least one bus adaptor to communicate between buses (see col. 12, lines 1-18).

5. Claims 33-34 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Laurenti (US No. 6,502,152) in view of Karamatas et al. (US Pub No. 2005/0060460).

In regard to claims 33, 34, Laurenti disclose the method for arbitrating the interrupt resources, comprising: determining a an interrupt range for an interrupt request (see col. 13, lines 56-67); determining an interrupt table entry for the interrupt range (see col. 13, lines 64 through col. 14, ine 11); and concurrently assigning the interrupt range and the interrupt table in response to the interrupt request and in view of available system resources (see col. 13, line 56 through col. 14, line 11). But Laurenti does not disclose the step of monitoring system performance and influencing interrupt assignment policy to tune the system performance. However Karamatas et al. disclose the interrupt assignment software 210 assigning interrupts for the I/O devices 206 among the nodes 202 in a performance optimized manner (see figure 2, para 24) including the monitoring (i.e. measuring) the system performance (see para 31) and influencing interrupt policy to tune system performance (see para 31-32) that would yield improved system performance. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Karamatas et al. within the system of Laurenti because it would

reduce the contention of the system's interconnect and yield improved system performance.

6. Claims 12-16, 19-20, 24-26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Laurenti in view of Short further in view of Bonola (US NO. 6,370,606).

In regard to claim 12, Laurenti and Short disclose the claimed subject matter as discussed above rejection except the teaching of the requesting component is a Plug and Play (PnP) manager that communicates with individual plug-in modules which decide which resources can be assigned to specific devices. However Bonola disclose the requesting component is a Plug and Play (PnP) manager that communicates with individual plug-in modules which decide which resources can be assigned to specific devices (see col. 5, lines 12-62) that facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Bonola within the system of Laurenti and Short because it would facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations.

In regard to claim 13, Bonola disclose further comprising a driver that supplies an arbiter to arbitrate interrupts (see col. 9, lines 6-64) that facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Bonola within the system of Laurenti and Short because

it would facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations.

In regard to claim 14, Bonola discloses the arbiter includes an interface associated with a function related to at least one of the following: testing/analyzing whether a possible set of resources operate (see col. 9, line 65 through col. 10, line 36); committing a specific set of resources that has been requested by a PnP manager (see col. 10, lines 9-46); querying for a set of devices that conflict with a resource set (see col. 11, lines 4-16); and marking resources that were in use by an operating system component when a machine is booted (see col. 11, lines 4-45) facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Bonola within the system of Laurenti and Short because it would facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations.

In regard to claim 15, Bonola discloses the arbiter is associated with a library function (se col. 12, lines 21-41) facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Bonola within the system of Laurenti and Short because it would facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations.

In regard to claim 16, Bonola discloses the library function is associated with a FindSuitableRange function that searches across available IRQs and

available IDT entries (see col. 12, lines 21-41) that facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Bonola within the system of Laurenti and Short because it would facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations.

In regard to claim 19, Bonola discloses the interrupt is a Message-Signaled Interrupts (MSI) (see col. 9, lines 39-65) that facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Bonola within the system of Laurenti and Short because it would facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations.

In regard to claim 20, Bonola discloses further comprising at least one of the following Application Programming Interfaces: IoConnectInterruptEx, and IoDisconnectInterruptEx, IRQ_ARBITER_INTERFACE (see col. 12, lines 21-34) that facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Bonola within the system of Laurenti and Short because it would facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations.

In regard to claim 24, Bonola discloses further comprising at least one local Advanced Programmable Interrupt Controller (APIC) that processes interrupts directed to a processor and an I/O APIC that collects interrupts from devices outside the processor (see col. 9, lines 56-65) that facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations . Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Bonola within the system of Laurenti and Short because it would facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations.

In regard to claim 25, Bonola discloses further comprising at least one of a link node to multiplex a plurality of interrupts (see col. 10, lines 25-36) that facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations . Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Bonola within the system of Laurenti and Short because it would facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations.

In regard to claim 26, Bonola discloses further comprising at least one user-mode component and at least one kernel-mode component to arbitrate an interrupt (see col. 4, lines 40-54) that facilitate the rapid development of a new generation of portable and intelligent I/O solutions for personal computers or workstations. Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Bonola within the system of Laurenti and Short because it would facilitate the rapid development

of a new generation of portable and intelligent I/O solutions for personal computers or workstations.

Allowable Subject Matter

7. Claims 28-32 are allowable over the prior of records.

8. The following is an Examiner's statement of reasons for the indication of allowable subject matter: Claim 28 is allowable over the prior art of record because the prior arts, cited in its entirety, or in combination, do not teach concurrently assigning the interrupt range and the interrupt table in response to the interrupt request, the interrupt request including a requested period of a resource's time.

The remaining claims, not specifically mentioned, are allowed for the same rationale as set forth their parent claims.

Response to Arguments

9. In view of remark filed on May 25, 2006, claims 1-27, 33-34 have been fully considered but they are not deemed to be persuasive.

In regard to claims 1-11, 17-18, 21-23, 27, Applicant(s) argue that ...Short et al. and Laurenti fail to teach or to suggest at least two dimensions related to an interrupt and an interrupt service component, at least one dimension including a time component.. (page 8). The Examiner does not agree. Short et al. teach the [interrupt] request including two dimensions (i.e. values) related to the interrupt that are (1) a limit which set a maximum number of pending interrupt and (2) a delay time (i.e. time component) which sets the maximum time interval that the interrupt controller will delay from the earliest pending interrupt event (see col. 3, lines 50-67).

In regard to claims 33-34, Applicant(s) argue that ...Karamatas et al. fail to teach or to suggest the time component in the request.. (page 9). The Examiner does not agree. Karamatas et al. teach the assignment of interrupt to the I/O including the time of responsiveness (see para 31).

Conclusion

10. Claims 1-27, 33-34 are rejected. Claims 28-32 are allowed.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (571) 272-3630. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Cottingham can be reached on (571) 272-7079 or via e-mail addressed to john.cottingham@uspto.gov. The fax phone number for this Group is (571) 273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**raymond.phan@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see hop://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 central telephone number is (571) 272-2100.

Raymond Phan
October 3, 2006